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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,456	ORION ET AL.	
	Examiner	Art Unit	
	Tonia LM Dollinger	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/24/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,12 and 14-36* is/are rejected.

7)☒ Claim(s) *5, 9-11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 31-36 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 31, "a computer readable storage medium containing computer readable instructions that when executed are operable to control a computer comprising" fails to comply with the written description requirement.

3. Claims 32-36 are rejected for incorporating the defects of claim 31.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless -

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21 (2) of such treaty in the English language.

6. Claims 1-4, 6, 12, 15-31 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Catherwood et al., US Patent 6,976,158 (herein after referred to as "Catherwood").

7. Referring to claim 1, Catherwood has taught a method of processing data comprising:

a. processing a function using a processor operable to perform a plurality of functions (Figure 4, column 2, line 7-column 3, line 24, A repeat instruction is the processing function.), said processor having interrupts enabled (Figure 3, element 365, Figure 4, element 440, Figure 5, element 580, Figure 6A, element 600, Column 2, line 7-column 3, line 24);

b. receiving an interrupt at said processor (Figure 4, elements 440 and 445) during processing of said function at a point at which a portion of said function has been processed (Figure 4, elements 440 and 445, When a repeatedly executing instruction, which has executed at least one time, is interrupted, then a portion of the function has been processed.);

c. suspending processing of said function (Figure 4, elements 440 and 445, column 2, line 58-column 3, line 24, column 8, lines 15-27);

d. accessing at least one control parameter, said at least one control parameter indicating whether processing of said function should be resumed from a point where it was interrupted or whether said function should be repeated from a start of said function following said interrupt (Figure 3, column 7, lines 35-46, The repeat status bit, element 345, is the control parameter that indicates whether to execute the repeat instruction

again from the start of the function or execute the next instruction in the program sequence after an interrupt.) such that said portion of said function that has already been processed is processed again (Figure 3, column 7, lines 35-46, The repeat status bit, element 345. When the repeat status bit is set, then the instruction to be repeated is processed again.);

e. following completion of said interrupt continuing processing of said function either at said start of said function or at said point at which it was interrupted dependent upon said control parameter (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, When the repeat status bit is set, then processing of the repeat function is performed again and the program counter is not incremented.).

8. Referring to claim 2, Catherwood has taught a method according to claim 1, as described above, and wherein said function processed by said processor may comprise an application, a system software routine, a thread, or multiple processing steps defined by software (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, The repeat instruction is a software routine with multiple steps.).

9. Referring to claim 3, Catherwood has taught a method according to claim 1, as described above, and comprising a further step of:

a. controlling said processor to store a restart address at which said processor should continue processing in dependence upon said at least one control parameter (column 7, lines 35-65, The program counter stores the restart address which depends on the loop control bit.).

10. Referring to claim 4, Catherwood has taught a method according to claim 3, wherein if said at least one control parameter indicates that said function is to be repeated following said interrupt said method comprises an additional step of:

a. accessing a further control parameter, said further control parameter being indicative of whether said function has idempotence or not (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, (Idempotence is interpreted as "a function that has repeatability when it is restarted. In other words it has not changed any state of the processor which would mean that the processor produced a different result if the function were repeated.", per the specification, paragraph [0009].) The repeat count register, 340, is the further control parameter. The repeat count register indicates repeatability. On an interrupt, when the repeat count register indicates the instruction needs to be repeated a number of times, then the state of the program counter does not change while executing the interrupt. When the repeat instruction finishes executing following the interrupt, then the program counter will be incremented to point to the next program instruction.); and
b. following completion of said interrupt continuing processing of said function at a start of said function if said further control parameter indicates said function to have idempotence or a fix-up routine to be performed before said function is restarted if said

control parameter indicates said function not to have idempotence (After an interrupt when the repeat instruction is finished executing, then program counter is fixed-up, or incremented, to point to the next instruction.).

11. Referring to claim 6, Catherwood has taught a method according to claim 1, as described above, and comprising a further step of:

a. controlling said processor to retrieve stored data relating to a restart address at which said processor should continue processing in dependence upon at least one control parameter (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, Instructions are fetched as indicated by the program counter, which is dependent on elements 340 and 345.);

b. following completion of said interrupt, continuing processing of said function from the stored restart address (column 7, lines 35-65, Following an interrupt the processing is resumed where the program counter indicates.).

12. Referring to claim 12, Catherwood has taught the method according to claim 7, as described above, and wherein said control parameter comprises a mode identifier (Figure 3, column 7, lines 35-46, The repeat status bit, element 345, is the control parameter that indicates the processor is operating in a repeat mode or a regular mode.).

13. Referring to claim 15, Catherwood has taught a method according to claim 1, as described above, and wherein if said at least one control parameter indicates that said

function should be resumed at a point that it was interrupted following processing of said interrupt, said processor stores an address at which the function was interrupted as a restart address in an exception register (Figure 3, element 365, Figure 4, element 440, Figure 5, element 580, Figure 6A, element 600, Column 2, line 7-column 3, line 24, The address to resume processing is stored in the program counter.), while if said control parameter indicates that said function should be restarted at a start of said function following processing of said interrupt, the exception register is not updated following said interrupt (Figure 3, element 365, Figure 4, element 440, Figure 5, element 580, Figure 6A, element 600, Column 2, line 7-column 3, line 24, When a repeat instruction is interrupted, then the program counter is not updated after the interrupt is finished.).

14. Referring to claim 16, Catherwood has taught an apparatus for processing data, said apparatus comprising:

a. a processor operable to perform a plurality of functions (Figure 4, column 2, line 7-column 3, line 24, A repeat is one of the plurality of functions.) and comprising:

b. a control parameter storage element operable to store a control parameter indicative of whether processing of a function should be resumed from a point where it was interrupted or whether it should be repeated following said interrupt (Figure 3, column 7, lines 35-46, The repeat status bit, element 345, is the control parameter that indicates whether to execute the repeat instruction again or execute the next instruction in the program sequence after an interrupt.);

c. an interrupt signal input port (Figure 3, element 365 inputs interrupt signals to element 355.);

d. an interrupt enable/disable selector (Figure 6A, elements 610, 620, 625, 630, 640, 645, and 650, Interrupts are selected based on priority.); and

e. function logic operable to control said processor to perform a function (Figure 4, column 2, line 7-column 3, line 24, A repeat instruction is the processing function.);

f. wherein said processor is operable to process function logic and in response to receipt of an interrupt signal during processing of said function at a point at which a portion of said function has been processed (Figure 4, elements 440 and 445, When a repeatedly executing instruction, which has executed at least one time, is interrupted, then a portion of the function has been processed.);

g. when said interrupt selector is enabled, to suspend processing of said function logic (Figure 4, elements 440 and 445, column 2, line 58-column 3, line 24, column 8, lines 15-27), and dependent on a value of said control parameter stored in said control parameter storage element to continue processing of said function either at a start of said function following said interrupt such that said portion of said function that has already been processed is processed again (Figure 3, column 7, lines 35-46, The repeat status bit, element 345. When the repeat status bit is set, then the instruction is processed again.) or at a point at which it was interrupted following completion of said interrupt (Figure 3, column 7, lines 35-46, The repeat status bit, element 345, is the control parameter that indicates whether to execute the repeat instruction again or

execute the next instruction in the program sequence after an interrupt.).

15. Claims 17-29 have nothing over claims 2-14, respectively, and are therefore rejected for the same reasons as set forth in claims 2-14.

16. Referring to claim 30, Catherwood has taught an apparatus for processing data according to claim 17, as described above, and wherein the processor comprising interrupt exception registers, said restart address storage element comprising an interrupt exception register (Figure 3, element 355).

17. Referring to claim 31, Catherwood has taught a computer program product comprising a computer readable storage medium containing computer readable instructions that when executed are operable to control a computer comprising:

a. function logic operable to control a processor to perform a function (Figure 4, column 2, line 7-column 3, line 24, A repeat instruction is the processing function.): and
b. disable interrupt logic operable to control said processor to disable interrupts (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, Once an interrupt in complete then the interrupt is disabled and normal execution resumes.);

18. c. wherein a first portion of said function logic operable to control said processor to perform a first portion of said function (Figure 4,.column 2, line 7-column 3, line 24, A repeat instruction is executed.), which has idempotence such that it does not alter a state of any part of the processor which would affect the repeatability of the function

(Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35The repeat function does not alter the program counter while it is executing,) and is operable to be executed by said processor before said disable interrupt logic (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, A repeat function executes and then an interrupt is enabled, the interrupt executes and the interrupt is disabled by disable interrupt logic. So the repeat function executes before the disable interrupt logic.) and a final portion of said function logic operable to control said processor to complete said function is operable to be executed after said disable interrupt logic is executed (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, Once the interrupt in complete then the interrupt is disabled and the repeat function resumes.).

19. Referring to claim 35, Catherwood has taught a computer program product according to claim 31, as described above, and said computer program product further comprising interrupt enable logic, said interrupt enable logic being operable to be performed before said function logic (Figure 3, column 7, lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, This happens during processor executions when an interrupt occurs before the repeat instruction executes.).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 7, 8, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Catherwood et al., US Patent 6,976,158 (herein after referred to as "Catherwood") in view of Anderson et al., US Patent 3,418,638 (herein after referred to as "Anderson").

22. Referring to claim 7, Catherwood has taught a method according to claim 6, as described above, and wherein said processor is operable in a plurality of modes (Interrupt mode, repeat mode, and regular processing mode to name a few.), said method comprising the additional steps of:

a. storing an address at which said processor switched mode (An address is stored in the program counter.). Catherwood has not specifically taught prior to initiation of processing of said function, switching said processor to a mode in which interrupts are automatically disabled on entry to said mode and on initiating said function, said function controlling said processor to enable interrupts. However, Anderson has taught prior to initiation of processing of said function, switching said processor to a mode in which interrupts are automatically disabled on entry to said mode; and on initiating said function, said function controlling said processor to enable interrupts (Figure 76, element 1188, Precise interrupt interlock) for the desirable purpose of preventing a

lower priority interrupt from interrupting a higher priority interrupt. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the method comprise the additional steps of switching said processor to a mode in which interrupts are automatically disabled on entry to said mode and on initiating said function, said function controlling said processor to enable interrupts, as taught by Anderson, to prevent a lower priority interrupt from interrupting a higher priority interrupt.

23. Referring to claim 8, Catherwood has taught t method according to claim 7, as described above, and wherein said at least one control parameter indicates that said restart address comprises said address at which the processor switched modes (column 7, lines 35-65, program counter).

24. Referring to claim 12, Catherwood has taught a method according to claim 7, as described above, and wherein said control parameter comprises a mode identifier (Figure 3, column 7, lines 35-46, The repeat status bit, element 345, is the control parameter that indicates the processor is operating in a repeat mode or a regular mode.).

25. Referring to claim 14, Catherwood has taught a method according to claim 1, as described above, and comprising the additional step of: following continuing of processing of said function, disabling interrupts (Figure 3, column 71 lines 35-46, column 2, line 58-column 3, line 24, column 8, lines 45-53, column 10, lines 15-16, column 11, lines 29-35, A repeat function executes and then an interrupt is enabled, the

interrupt executes and the interrupt is disabled by disable interrupt logic. So the repeat function executes before the interrupts are disabled.).

Response to Arguments

26. Applicant's arguments filed January 24, 2008 have been fully considered but they are not persuasive.

27. On page 16, Applicant argues in essence:

> *"It is noted that Catherwood does not disclose interrupting a function at a point at which a portion of the function has been processed and then either processing this portion again following the interrupt or processing the function at the point at which it was interrupted. In Catherwood, although a repeat instruction may be interrupted at a point at which a portion of the function, for example, three of eight repeat instructions have been processed, when the function is restarted it will always restart to process only the final five instructions. In other words, in Catherwood it will always resume from a point at which it was interrupted and it will never process those parts of the function that have already been processed, i.e., in the example above the first three repeat functions. "*

However, an instruction that is repeated is the exact same instruction being repeated over and over again. If an instruction is repeated eight times, then the same instruction is executed the first time up until the eighth time. So in Catherwood, when an instruction or portion is repeated, then the instruction or portion is repeated again. So Catherwood has taught the limitations of the claims. Therefore this argument is moot.

28. On page 17, Applicant argues in essence:

> *"There is no motivation for combining the Catherwood and Anderson references even if they did teach the subject matter of applicants' independent claim 1 and claims 7, 8, 12 and 14 dependent thereon."*

However, Catherwood and Anderson has taught claims 7, 8, 12 and 14. Furthermore the motivation to combine Anderson with Catherwood is to prevent

a lower priority interrupts from interrupting higher priority interrupts. Also see the rejection above. Therefore this argument is moot.

Allowable Subject Matter

29. Claim 5, 9-11 and 13, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

30. No art has been applied to claims 32-34 and 36. Only 112 rejections have been made above to the claims.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia LM Dollinger whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLMD

/Tonia LM Dollinger/
Primary Examiner, Art Unit 2181